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(54) **PIXEL CIRCUIT AND ORGANIC LIGHT-EMITTING DISPLAY COMPRISING THE SAME**

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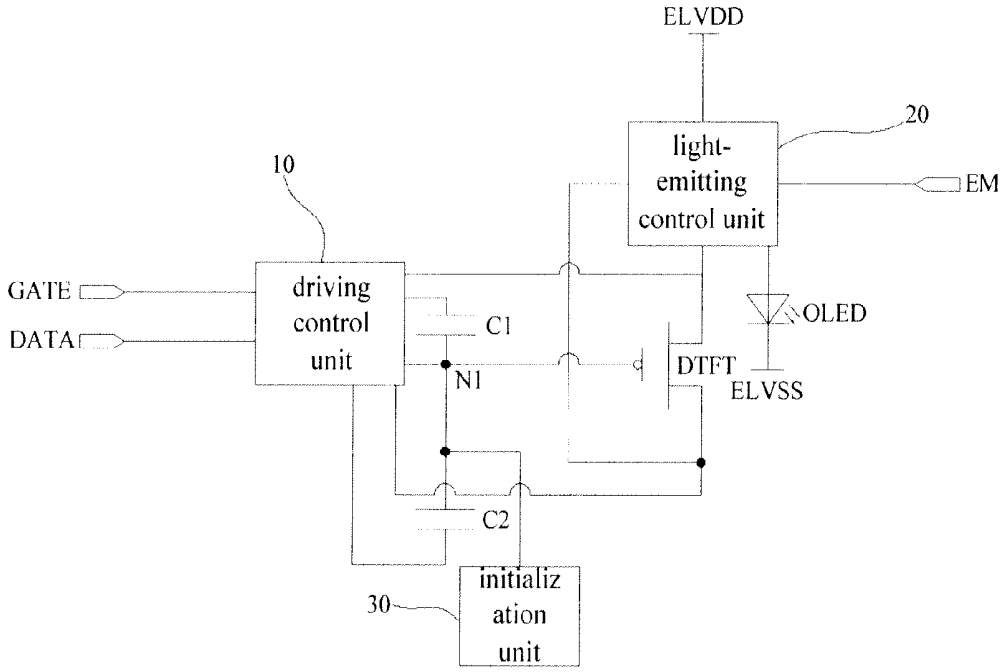
(57) **ABSTRACT**

Provided are a pixel circuit and an organic light-emitting display. The pixel circuit comprises a driving thin film transistor and a light-emitting diode which is connected between a low level input terminal and a high level input terminal of a driving power supply in series, the pixel circuit further comprises a first capacitor and a driving control unit, a first terminal of the first capacitor is electrically connected with a first electrode of the driving thin film transistor through the driving control unit, a second terminal of the first capacitor is connected with a gate of the driving thin film transistor, a second electrode of the driving thin film transistor is electrically connected with the gate of the driving thin film transistor through the driving control unit, the driving control unit is connected with a gate line and a data line. Since respective pixel circuits may output uniform currents, the brightness of light-emitting diodes in the pixel circuits is uniform, and in turn the display brightness of the organic light-emitting display comprising the pixel circuits is uniform.



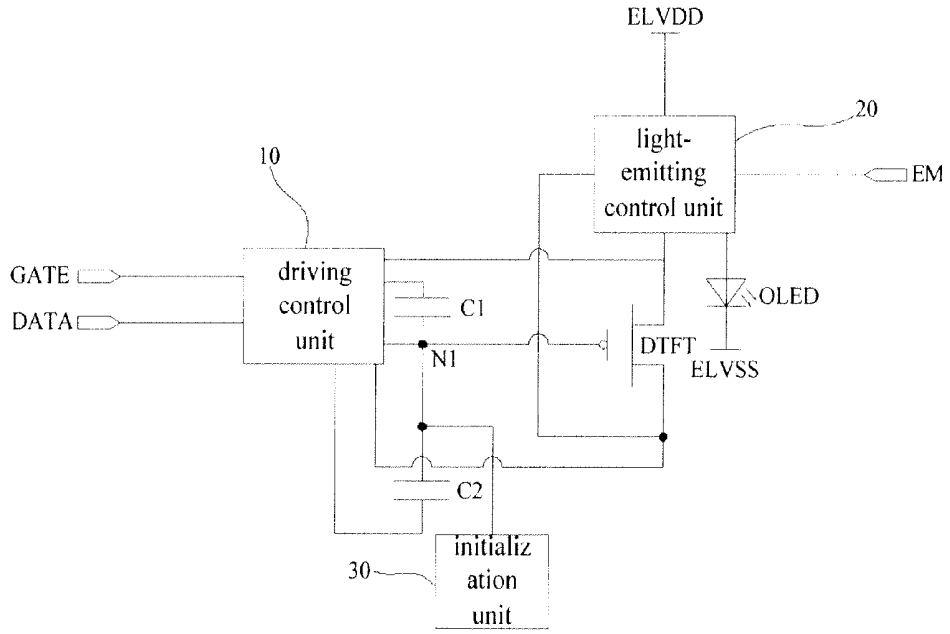
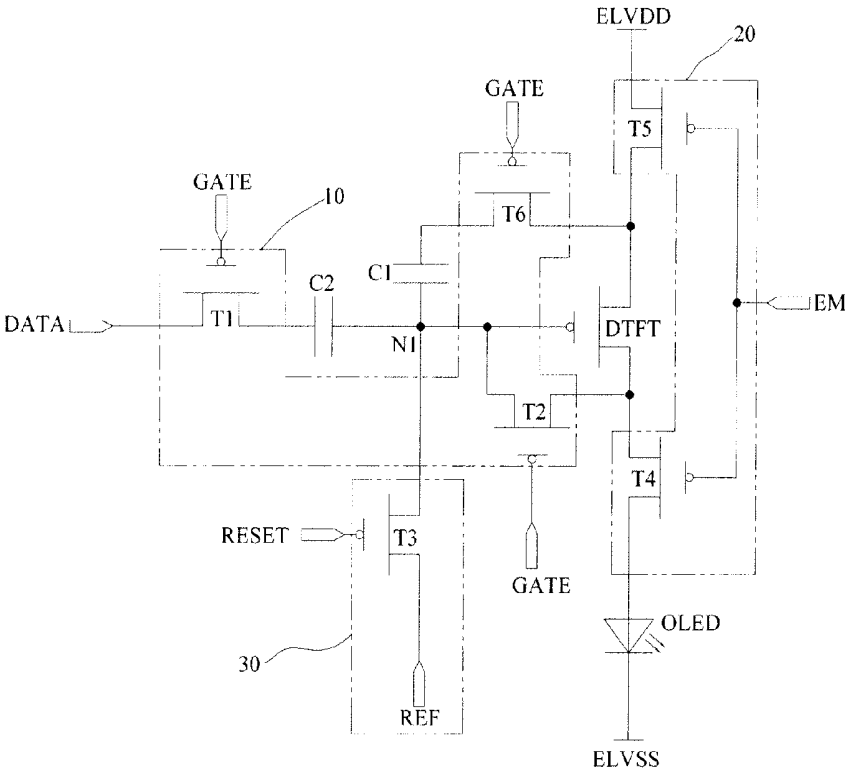

ELVDD
20
light-
emitting
control unit
EM
10
GATE
DATA
driving
control
unit
C1
N1
OLED
DTFT
ELVSS
C2
30
initializ
ation
unit

Fig.1


ELVDD
20
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T5
GATE
10
T6
C2
C1
DATA
T1
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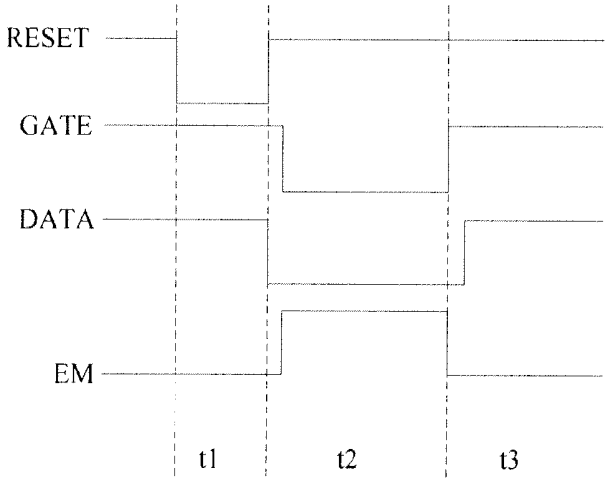
EM
T2
T4
RESET
T3
GATE
OLED
30
REF
ELVSS

Fig. 2


RESET
GATE
DATA
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t1
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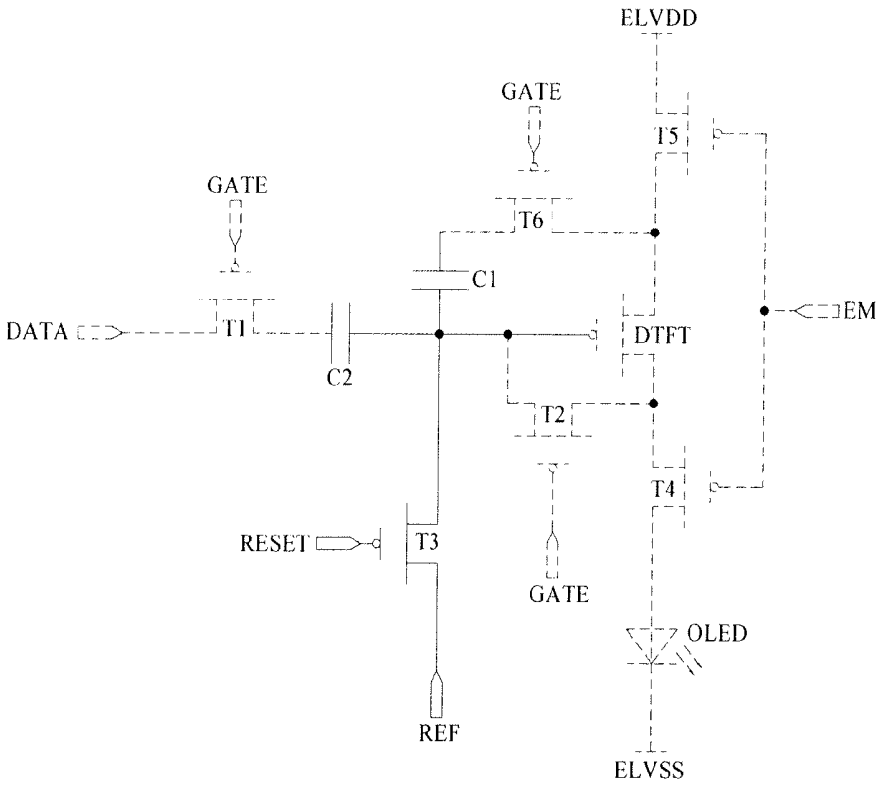
Fig. 3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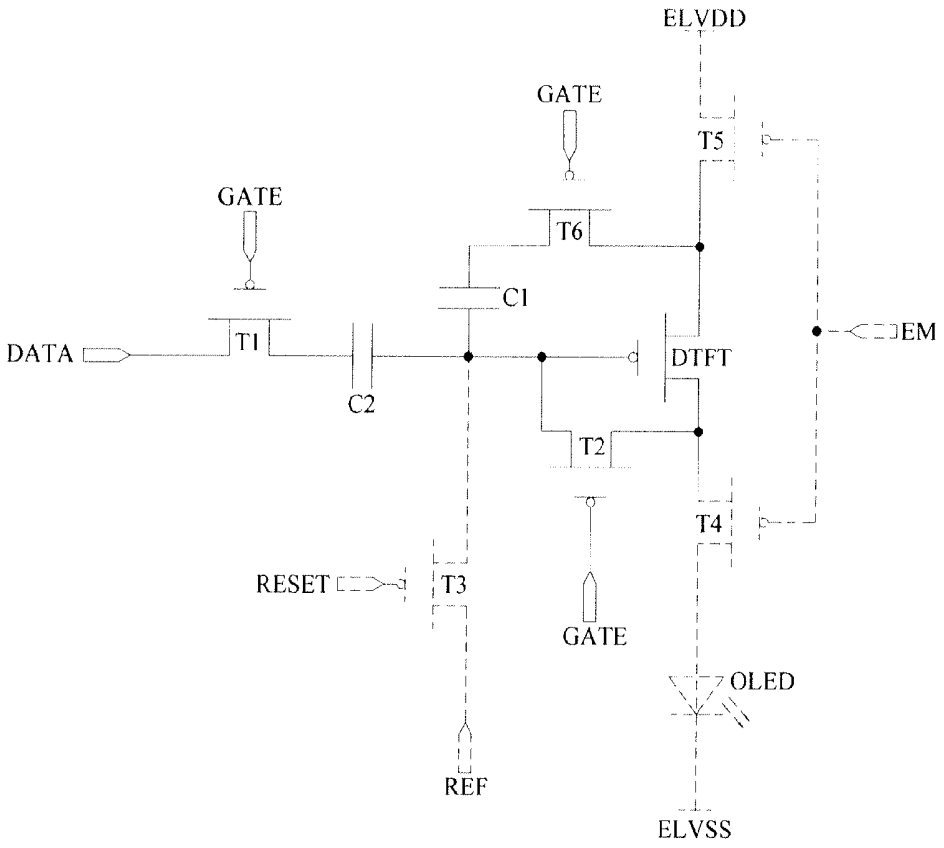
ELVSS

Fig. 4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OLED
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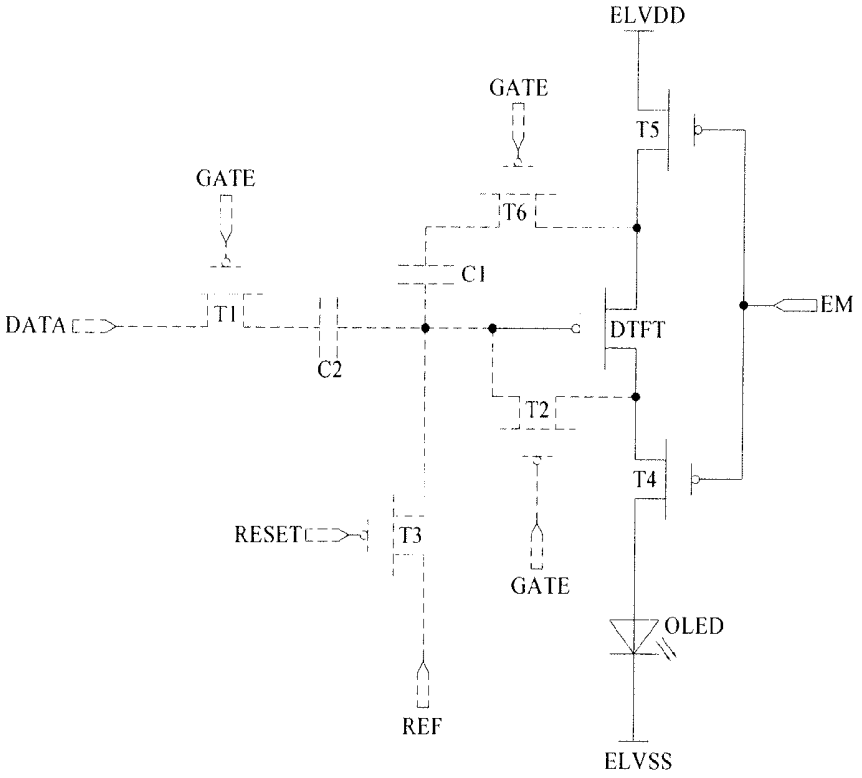
ELVSS

Fig.5


ELVDD
GATE
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GATE
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T3
GATE
OLED
REF
ELVSS

Fig.6

PIXEL CIRCUIT AND ORGANIC LIGHT-EMITTING DISPLAY COMPRISING THE SAME

TECHNICAL FIELD

[0001] The present disclosure relates to a field of organic light-emitting display, and particularly to a pixel circuit and an organic light-emitting display comprising the same.

BACKGROUND

[0002] In an Active Matrix Organic Light Emitting Diode (AMOLED) display panel, the emission brightness of an OLED (Organic Light Emitting Diode) is directly proportional to an amplitude of a driving current supplied thereto. A great driving current is required to realize an optimal display effect. A Low Temperature Poly-Silicon technique has become an optimal selection for the AMOLED display panel because it may provide a high mobility. However an inherent problem of shifts in threshold voltages Vth of thin film transistors existed in the Low Temperature Poly-Silicon technique may cause non-uniformity in currents output from respective pixel circuits, such that the display brightness is also non-uniform.

[0003] Therefore, how to improve the uniformity in the currents output from the respective pixel circuits is a technical problem needed to be settled urgently in the art.

SUMMARY

[0004] An object of the present disclosure is to provide a pixel circuit and an organic light-emitting display comprising the same. Respective pixel circuits may output uniform currents, so that the brightness of light-emitting diodes in the respective pixel circuits may be uniform, and in turn the organic light-emitting display comprising the pixel circuits may have a uniform display brightness.

[0005] According to an aspect of the present disclosure, there is provided a pixel circuit comprising a driving thin film transistor and a light-emitting diode which is connected between a low level input terminal and a high level input terminal of a driving power supply in series, wherein the pixel circuit further comprises a first capacitor and a driving control unit, a first terminal of the first capacitor is electrically connected with a first electrode of the driving thin film transistor through the driving control unit, a second terminal of the first capacitor is connected with a gate of the driving thin film transistor, a second electrode of the driving thin film transistor is electrically connected with the gate of the driving thin film transistor through the driving control unit, the driving control unit is connected with a gate line and a data line, and during a data writing stage, the driving control unit controls to connect the first terminal of the first capacitor to the first electrode of the driving thin film transistor and connect the gate of the driving thin film transistor to the second electrode of the driving thin film transistor, such that the driving thin film transistor is turned on.

[0006] Optionally, the pixel circuit may further comprise a second capacitor, a first terminal thereof is connected with the second terminal of the first capacitor, and a second terminal thereof is electrically connected with the data line through the driving control unit.

[0007] Optionally, the driving control unit may further comprise a first driving control transistor, a gate thereof is connected with the gate line, a first electrode thereof is connected with the data line, and a second electrode thereof is connected with the second terminal of the second capacitor.

[0008] Optionally, the pixel circuit may further comprise an initialization unit for providing a low level and connected to the second terminal of the first capacitor and the first terminal of the second capacitor.

[0009] Optionally, the initialization unit may comprise an initialization transistor, a first electrode thereof is connected with the second terminal of the first capacitor and the first terminal of the second capacitor, a second electrode thereof is connected with the low level input terminal, and a gate thereof is connected with a reset signal input terminal.

[0010] Optionally, the driving control unit may comprise a second driving control transistor and a third driving control transistor, a gate of the second driving control transistor is connected with the gate line, a first electrode of the second driving control transistor is connected with the second electrode of the driving thin film transistor, a second electrode of the second driving control transistor is connected with the gate of the driving thin film transistor, a gate of the third driving control transistor is connected with the gate line, a first electrode of the third driving control transistor is connected with the first terminal of the first capacitor, and a second electrode of the third driving control transistor is connected with the first electrode of the driving thin film transistor.

[0011] Optionally, the pixel circuit may further comprise a light-emitting control unit which is connected with a light-emitting control line and is capable of connecting the high level input terminal of the driving power supply to the first electrode of the driving thin film transistor, and/or connecting the low level input terminal of the driving power supply to the second electrode of the driving thin film transistor, according to a signal supplied from the light-emitting control line.

[0012] Optionally, the light-emitting control unit may comprise a first light-emitting control transistor and a second light-emitting control transistor, a gate of the first light-emitting control transistor is connected with the light-emitting control line, a first electrode of the first light-emitting control transistor is connected with the first electrode of the driving thin film transistor, a second electrode of the first light-emitting control transistor is connected with the high level input terminal of the driving power supply, a gate of the second light-emitting control transistor is connected with the light-emitting control line, a first electrode of the second light-emitting control transistor is connected with the second electrode of the driving thin film transistor, a second electrode of the second light-emitting control transistor is connected with an anode of the light-emitting diode, and a cathode of the light-emitting diode is connected with the low level input terminal of the driving power supply.

[0013] Optionally, the driving thin film transistor, the first driving control transistor, the second driving control transistor, the third driving control transistor, the initialization transistor, the first light-emitting control transistor and the second light-emitting control transistor are all P-type transistors.

[0014] According to another aspect of the present disclosure, there is further provided an organic light-emitting display, wherein the organic light-emitting display comprises the above pixel circuit according to the present disclosure.

[0015] In the pixel circuit according to the present disclosure, during the data writing stage of the pixel circuit, the driving control unit controls to connect the first terminal of the first capacitor to the first electrode of the driving thin film

transistor and connect the gate of the driving thin film transistor to the second electrode of the driving thin film transistor, thus the driving thin film transistor actually forms a diode being in a critical conduction state at this time. A gate voltage V_g of the driving thin film transistor may be a difference obtained by subtracting a threshold voltage $V_{th,DTFT}$ of the driving thin film transistor from a voltage V_{N1} at the second terminal of the first capacitor (that is, $V_g=V_{N1}-V_{th,DTFT}$). During this data writing stage, the first capacitor records the gate voltage of the driving thin film transistor and holds it till a light-emitting stage of the light-emitting diode in the pixel circuit. During the light-emitting stage of the light-emitting diode OLED in the pixel circuit, the driving thin film transistor is in a saturation state, the gate voltage of the driving thin film transistor is the voltage held on the first capacitor, that is, $V_{N1}-V_{th,DTFT}$, and a voltage V_{gs} between the gate and the first electrode of the driving thin film transistor is a difference between a voltage V_{dd} input from the first electrode of the driving thin film transistor and the gate voltage of the driving thin film transistor, that is, $V_{gs}=V_{dd}-(V_{N1}-V_{th,DTFT})$. An equation for calculating a drain current of the driving thin film transistor is as follows:

$$I_d = \frac{1}{2}\mu C_{ox}(W/L)(|V_{gs,DTFT}| - |V_{th,DTFT}|)^2$$
$$= \frac{1}{2}\mu C_{ox}(W/L)[V_{dd} - (V_{N1} - V_{th,DTFT}) - V_{th,DTFT}]^2$$
$$= \frac{1}{2}\mu C_{ox}(W/L)(V_{dd} - V_{N1})^2.$$

[0016] It can be seen from the above equation that the drain current of the driving thin film transistor is independent of the threshold voltage of the driving thin film transistor (in other words, the threshold voltage of the driving thin film transistor is compensated) during the light-emitting stage of the light-emitting diode, so that the problems of non-uniform brightness and brightness decay in the AMOLED panel are settled.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Drawings, which constitute a part of the specification, are provided to assistant to further understand the present disclosure and are used to explain the present disclosure together with following detailed implementations, but should not be constructed as limitations on the present disclosure. Wherein:

[0018] FIG. **1** is a circuit diagram illustrating a first implementation of a pixel circuit according to the present disclosure;

[0019] FIG. **2** is a circuit diagram illustrating a second implementation of the pixel circuit according to the present disclosure;

[0020] FIG. **3** is a timing diagram of control signals in the pixel circuit according to the present disclosure;

[0021] FIG. **4** is an equivalent circuit diagram of the pixel circuit shown in FIG. **2** during a t**1** stage;

[0022] FIG. **5** is an equivalent circuit diagram of the pixel circuit shown in FIG. **2** during a t**2** stage; and

[0023] FIG. **6** is an equivalent circuit diagram of the pixel circuit shown in FIG. **2** during a t**3** stage.

[0024]

Reference Signs	
10: driving control unit	20: light-emitting control unit
30: initialization unit	EM: light-emitting control line
C1: first capacitor	C2: second capacitor
T1: first driving control transistor	T2: second driving control transistor
T3: initialization transistor	T4: second light-emitting control transistor
T5: first light-emitting control transistor	T6: third driving control transistor
DTFT: driving thin film transistor	OLED: light-emitting diode
GATE: gate line	DATA: data line
ELVDD: high level input terminal of a driving power supply	
ELVSS: low level input terminal of the driving power supply	
RESET: reset signal input terminal	

DETAILED DESCRIPTION

[0025] Detailed implementations of the present disclosure will be described in details below in connection with the drawings. It should be understood that the detailed implementations described herein are only used for illustrating and explaining the present disclosure, instead of limiting the present disclosure.

[0026] In embodiments of the present disclosure, there is provided a pixel circuit, as illustrated in FIG. **1**, the pixel circuit comprises a driving thin film transistor DTFT and a light-emitting diode OLED which is connected between a low level input terminal ELVSS and a high level input terminal ELVDD of a driving power supply in series.

[0027] In an example, the pixel circuit further comprises a first capacitor C**1** and a driving control unit **10**, a first terminal of the first capacitor C**1** is electrically connected with a first electrode (one of a source and a drain of the driving thin film transistor DTFT) of the driving thin film transistor DTFT through the driving control unit **10**, a second terminal of the first capacitor C**1** is connected with a gate of the driving thin film transistor DTFT, a second electrode (the other of the source and the drain of the driving thin film transistor DTFT) of the driving thin film transistor DTFT is electrically connected with the gate of the driving thin film transistor DTFT through the driving control unit **10**, the driving control unit **10** is connected with a gate line GATE and a data line DATA, and during a data writing stage (that is, a t**2** stage in FIG. **3**), the driving control unit **10** controls to connect the first terminal of the first capacitor C**1** to the first electrode of the driving thin film transistor DTFT and connect the gate of the driving thin film transistor DTFT to the second electrode of the driving thin film transistor DTFT, and further controls to turn on the driving thin film transistor DTFT.

[0028] Those skilled in the art should understand that the first electrode and the second electrode of the driving thin film transistor DTFT are connected between the low level input terminal ELVSS and the high level input terminal ELVDD of the driving power supply in series. During other stages except for the data writing stage, the gate of the driving thin film transistor DTFT is disconnected from the first electrode of the driving thin film transistor DTFT, and the gate of the driving thin film transistor DTFT is also disconnected from the second electrode of the driving thin film transistor DTFT.

[0029] During the data writing stage, signals input from the gate line GATE and the data line DATA are active (as illustrated in FIG. **3**), the driving control unit **10** enables to con-

nect the first terminal of the first capacitor C1 to the first electrode of the driving thin film transistor DTFT and connect the gate of the driving thin film transistor DTFT to the second electrode of the driving thin film transistor DTFT, thus the driving thin film transistor DTFT actually forms a diode being in a critical conduction state at this time, and the threshold voltage $V_{th,DTFT}$ of the driving thin film transistor DTFT at this time is recorded and stored by the first capacitor C1.

[0030] A gate voltage of the driving thin film transistor DTFT is $V_{N1}-V_{th,DTFT}$ at this time, herein V_{N1} refers to a voltage at a node N1 at which the second terminal of the first capacitor C1 is connected to the data line DATA, and V_{N1} is independent of the threshold voltage $V_{th,DTFT}$ of the driving thin film transistor DTFT. During a light-emitting stage of the light-emitting diode OLED (that is, a t3 stage in FIG. 3), the gate voltage $V_{N1}-V_{th,DTFT}$ of the driving thin film transistor DTFT is held by the first capacitor C1, therefore a current I_d flowing through the first electrode of the driving thin film transistor DTFT and the second electrode of the driving thin film transistor DTFT (that is, a current flowing through the source and the drain of the driving thin film transistor) is as follows:

$$I_d = \frac{1}{2}\mu C_{ox}(W/L)(|V_{gs,DTFT}| - |V_{th,DTFT}|)^2$$
$$= \frac{1}{2}\mu C_{ox}(W/L)[V_{dd} - (V_{N1} - V_{th,DTFT}) - V_{th,DTFT}]^2$$
$$= \frac{1}{2}\mu C_{ox}(W/L)(V_{dd} - V_{N1})^2,$$

[0031] wherein μ is a field effect mobility of the driving thin film transistor DTFT; C_{ox} is a capacitance value of an unit area in an insulation layer at the gate of the driving thin film transistor DTFT; W is a channel width of the driving thin film transistor DTFT; L is a channel length of the driving thin film transistor DTFT; and V_{dd} is a voltage input from the high level input terminal of the driving power supply.

[0032] It can be seen from above that the current I_d flowing through the first electrode of the driving thin film transistor DTFT and the second electrode of the driving thin film transistor DTFT is independent of the threshold voltage $V_{th,DTFT}$ of the driving thin film transistor DTFT. Therefore a shift in the threshold voltage $V_{th,DTFT}$ of the driving thin film transistor DTFT would not affect a current output from the driving thin film transistor DTFT (that is, a drain current of the driving thin film transistor DTFT), so that the brightness of the light-emitting diode OLED would not be affected.

[0033] In an example, the pixel circuit may further comprise a second capacitor C2, a first terminal thereof is connected with the second terminal of the first capacitor C1, and a second terminal thereof is electrically connected with the data line DATA through the driving control unit 10.

[0034] During the data writing stage (that is, the t2 stage shown in FIG. 3), the data line DATA charges the second capacitor C2 through the driving control unit 10. During the light-emitting stage of the light-emitting diode OLED (that is, the t3 stage shown in FIG. 3), the second capacitor C2 insulates the gate of the driving thin film transistor DTFT from the data line DATA so as to prevent a current leakage.

[0035] In order to further prevent the current leakage of the gate of the driving thin film transistor DTFT during the light-emitting stage of the light-emitting diode OLED (the t3 stage), in an example, the driving control unit 10 may further comprise a first driving control transistor T1.

[0036] A gate of the first driving control transistor T1 is connected with the gate line GATE, a first electrode thereof (one of a source and a drain of the first driving control transistor T1) is connected with the data line DATA, and a second electrode thereof (the other of the source and the drain of the first driving control transistor T1) is connected with the second terminal of the second capacitor C2.

[0037] During the data writing stage (that is, the t2 stage shown in FIG. 3), the signal of the gate line GATA and the signal of the data line DATA are active, the first driving control transistor T1 is turned on (the first electrode and the second electrode of the first driving control transistor T1 are connected with each other), the data line DATA charges the second capacitor C2 through the first driving control transistor T1. During the light-emitting stage of the light-emitting diode OLED (that is, the t3 stage shown in FIG. 3), the first driving control transistor T1 is turned off (that is, the source and the drain of the first driving control transistor T1 is disconnected from each other), so that the current leakage of the gate of the driving thin film transistor DTFT to the data line DATA may be prevented.

[0038] In order to eliminate an affect on the driving thin film transistor DTFT by residual quantity of electric charges on the first capacitor C1 and the second capacitor C2, in an example, the pixel circuit may further comprise an initialization unit 30 for providing a low level.

[0039] The initialization unit 30 is electrically connected to a common terminal of the first capacitor C1 and the second capacitor C2, the second terminal of the first capacitor C1 and the first terminal of the second capacitor C2 form the common terminal. Before the data writing stage (that is, before the t2 stage shown in FIG. 3), an initialization stage (that is, a t1 stage shown in FIG. 3) may be performed at first, so that the first capacitor C1 and the second capacitor C2 are discharged by the initialization unit 30, in order to complete an initialization of the pixel circuit.

[0040] In particular, as illustrated in FIG. 2, the initialization unit 30 may comprise an initialization transistor T3, a first electrode thereof (one of a source and a drain of the initialization transistor T3) is connected between the second terminal of the first capacitor C1 and the first terminal of the second capacitor C2, a second electrode thereof (the other of the source and the drain of the initialization transistor T3) is connected with a low level input terminal REF (this low level input terminal REF may provide the low level), and a gate thereof is connected with a reset signal input terminal RESET. During the initialization stage (the t1 stage), a reset signal input from the reset signal input terminal RESET is active, the initialization transistor T3 is turned on so as to discharge the first capacitor C1 and the second capacitor C2, thus a state initialization of the pixel circuit is completed.

[0041] As a detailed implementation, in an example, as illustrated in FIG. 2, the driving control unit 10 may further comprise a second driving control transistor T2 and a third driving control transistor T6.

[0042] A gate of the second driving control transistor T2 is connected with the gate line GATE, a first electrode of the second driving control transistor T2 (one of a source and a drain of the second driving control transistor T2) is connected with the second electrode of the driving thin film transistor DTFT, a second electrode of the second driving control transistor T2 (the other of the source and the drain of the second

driving control transistor T2) is connected with the gate of the driving thin film transistor DTFT, a gate of the third driving control transistor T6 is connected with the gate line GATE, a first electrode of the third driving control transistor T6 (one of a source and a drain of the third driving control transistor T6) is connected with the first terminal of the first capacitor C1, and a second electrode of the third driving control transistor T6 (the other of the source and the drain of the third driving control transistor T6) is connected with the first electrode of the driving thin film transistor DTFT.

[0043] During the data writing stage (that is, the t2 stage shown in FIG. 3), the signals from the gate line GATE and the data line DATA are active, the second driving control transistor T2 and the third driving control transistor T6 are turned on, so that the driving thin film transistor DTFT forms a diode. During the initialization stage (that is, the t1 stage shown in FIG. 3) and the light-emitting stage of the light-emitting diode OLED (the t3 stage), the second driving control transistor T2 and the third driving control transistor T6 are turned off.

[0044] As described above, the light-emitting diode OLED is connected between the low level input terminal ELVSS and the high level input terminal ELVDD of the driving power supply in series, and the first electrode and the second electrode of the driving thin film transistor DTFT are also connected between the low level input terminal ELVSS and the high level input terminal ELVDD of the driving power supply in series. When the driving thin film transistor DTFT is turned on, the current may flow to the low level input terminal ELVSS of the driving power supply to the high level input terminal ELVDD of the driving power supply so as to flow through the light-emitting diode OLED and drive the light-emitting diode OLED to emit light.

[0045] In order to facilitate controlling of the light-emitting diode OLED, as illustrated in FIG. 2, generally the pixel circuit may further comprise a light-emitting control unit 20, which is connected with a light-emitting control line EM and may connect the high level input terminal ELVDD of the driving power supply to the first electrode of the driving thin film transistor DTFT and/or connect the low level input terminal ELVSS of the driving power supply to the second electrode of the driving thin film transistor DTFT, according to a signal supplied from the light-emitting control line EM.

[0046] During the light-emitting stage of the light-emitting diode OLED (that is, the t3 stage shown in FIG. 3), only a signal from the light-emitting control line EM is active, and the driving thin film transistor DTFT is disconnected with both of the gate line GATE and the data line DATA at this time. Since the first capacitor C1 holds the gate voltage of the driving thin film transistor DTFT, the driving thin film transistor DTFT is in a conduction state. Also, since the signal from the light-emitting control line EM is active, the current supplied from the driving power supply may flow to the low level input terminal ELVSS from the high level input terminal ELVDD, so that the light-emitting diode OLED may emit light.

[0047] During other stages except for the light-emitting stage of the light-emitting diode OLED (that is, the t3 stage shown in FIG. 3), the high level input terminal ELVDD and the low level input terminal ELVSS of the driving power supply are disconnected with each other, therefore the light-emitting diode OLED does not emit light.

[0048] As a detailed implementation, as illustrated in FIG. 2, the light-emitting control unit 20 may comprise a first light-emitting control transistor T5 and a second light-emitting control transistor T4, a gate of the first light-emitting control transistor T5 is connected with the light-emitting control line EM, a first electrode of the first light-emitting control transistor T5 (one of a source and a drain of the first light-emitting control transistor T5) is connected with the first electrode of the driving thin film transistor DTFT, a second electrode of the first light-emitting control transistor T5 (the other of the source and the drain of the first light-emitting control transistor T5) is connected with the high level input terminal ELVDD of the driving power supply, a gate of the second light-emitting control transistor T4 is connected with the light-emitting control line EM, a first electrode of the second light-emitting control transistor T4 (one of a source and a drain of the second light-emitting control transistor T4) is connected with the second electrode of the driving thin film transistor DTFT, a second electrode of the second light-emitting control transistor T4 (the other of the source and the drain of the second light-emitting control transistor T4) is connected with an anode of the light-emitting diode OLED, and a cathode of the light-emitting diode OLED is connected with the low level input terminal ELVSS of the driving power supply.

[0049] In another embodiment of the present disclosure, the light-emitting diode OLED may further be connected between the first electrode of the first light-emitting control transistor T5 and the first electrode of the driving thin film transistor DTFT in series.

[0050] In a case that the signal of the light-emitting control line EM is active, the first light-emitting control transistor T5 and the second light-emitting control transistor T4 are both turned on, the current may flow to the low level input terminal ELVSS of the driving power supply from the high level input terminal ELVDD of the driving power supply, so that the light-emitting diode OLED may emit light.

[0051] During the other stages (that is, the t1 stage and the t2 stage shown in FIG. 3) except for the light-emitting stage of the light-emitting diode OLED (that is, the t3 stage shown in FIG. 3), the first light-emitting control transistor T5 is turned off, the high level input terminal ELVDD of the driving power supply is disconnected from the first electrode of the driving thin film transistor DTFT, so that a high level of the high level input terminal ELVDD of the driving power supply is prevented from affecting the first electrode of the driving thin film transistor DTFT.

[0052] During the data writing stage (that is, the t2 stage shown in FIG. 3), because the gate of the driving thin film transistor DTFT is connected with the second electrode of the driving thin film transistor DTFT, the driving thin film transistor DTFT actually forms a diode being in a critical conduction state at this time, therefore the second light-emitting control transistor T4 is turned off, so that a current leakage current from the driving thin film transistor DTFT may be prevented from flowing to the light-emitting diode OLED.

[0053] In the present disclosure, no limitation is made for types of the driving thin film transistor DTFT, the first driving control transistor T1, the second driving control transistor T2, the third driving control transistor T6, the initialization transistor T3, the first light-emitting control transistor T5 and the second light-emitting control transistor T4. However, the first driving control transistor T1, the second driving control transistor T2 and the third driving control transistor T3 should have a same type (all being P-type or all being N-type), while the first light-emitting control transistor T5 and the second

light-emitting control transistor T4 should have a same type (all being P-type or all being N-type).

[0054] In the implementation illustrated in FIG. **2** of the present disclosure, the driving thin film transistor DTFT, the first driving control transistor T**1**, the second driving control transistor T**2**, third driving control transistor T**6**, the initialization transistor T**3**, the first light-emitting control transistor T**5** and the second light-emitting control transistor T**4** are all P-type transistors. Active signals for the gate line GATE, the date line DATA and the light-emitting control line EM are the low level signal.

[0055] An operation principle of an implementation according to the present disclosure will be discussed below in connection with FIGS. **2**, **4**-**6**.

[0056] FIG. **4** illustrates an equivalent circuit diagram of the pixel circuit shown in FIG. **2** during the initialization stage (that is, the t**1** stage shown in FIG. **3**), wherein parts drawn with solid lines denote powered-on parts while parts drawn with dotted lines denote powered-off parts.

[0057] During the initialization stage, the reset signal input terminal RESET supplies the initialization transistor T**3** with an active signal in order to turn on the initialization transistor T**3**, so that the residual quantity of electric charges in the first capacitor C**1** and the second capacitor C**2** flow to the low level input terminal REF. At this time, the gate voltage of the driving thin film transistor DTFT is a voltage V_{ref} provided from the low level input terminal REF, and a voltage at the first terminal of the second capacitor C**2** is also the voltage V_{ref} provided from the low level input terminal REF.

[0058] FIG. **5** illustrates an equivalent circuit diagram of the pixel circuit shown in FIG. **2** during the data writing stage (that is, the t**2** stage shown in FIG. **3**), similar to the FIG. **4**, parts drawn with solid lines denote powered-on parts while parts drawn with dotted lines denote powered-off parts.

[0059] During the data writing stage (that is, the t**2** stage shown in FIG. **3**), the signal input from the reset signal input terminal RESET jumps to a high level, the initialization transistor T**3** is turned off, and the first capacitor C**1** holds the voltage V_{ref} provided from the low level input terminal REF. At the same time, the signal of the gate line GATE is active, the first driving control transistor T**1** is turned on, the data line DATA writes a display data signal into the pixel circuit, at this time, a voltage at the node N**1** being the first terminal of the second capacitor C**2** is a sum of a voltage V_{data} of the data line DATA and the voltage V_{ref} provided from the low level input terminal REF, that is, $V_{data}+V_{ref}$. At a same time, because the signal of the gate line GATE is active, the second driving control transistor T**2** is turned on, so that the gate of the driving thin film transistor DTFT is connected with the second electrode of the driving thin film transistor DTFT, and the driving thin film transistor DTFT actually forms a diode being in a critical conduction state at this time, thus the threshold voltage $V_{th,DTFT}$ of the driving thin film transistor DTFT is held and recorded by the first capacitor C**1**. At this time, the gate voltage of the driving thin film transistor is $V_{data}+V_{ref}-V_{th,DTFT}$ and is stored by the first capacitor C**1**.

[0060] During the data writing stage (that is, the t**2** stage shown in FIG. **3**), the light-emitting control line EM is in a high level, the second light-emitting control transistor T**4** is turned off, thus an action for writing the data into the pixel would not affect a light-emitting state of the light-emitting diode OLED, which may avoid flickers in the display. At the same time, the high level of the light-emitting control line EM ensures that the first light-emitting control transistor T**5** is turned off, ensures that the driving thin film transistor DTFT is disconnected from the high level input terminal ELVDD of the driving power supply at this moment, which may avoid a harmful effect on the gate voltage of the driving thin film transistor DTFT caused by the current leakage of the driving thin film transistor DTFT. On the other hand, the signal of the gate line GATE is active, the third driving control transistor T**6** is turned on, so that the first electrode of the driving thin film transistor DTFT is prevented from being float, and the third driving control transistor T**6** may introduce the gate voltage of the driving thin film transistor DTFT to the first electrode of the driving thin film transistor DTFT, thus the gate voltage of the driving thin film transistor DTFT would not be affected even if a current leakage phenomenon occurs in the driving thin film transistor DTFT.

[0061] FIG. **6** illustrates an equivalent circuit diagram of the pixel circuit shown in FIG. **2** during the light-emitting stage of the light-emitting diode OLED (that is, the t**3** stage shown in FIG. **3**), as similar to FIGS. **4** and **5**, parts drawn with solid lines denote powered-on parts while parts drawn with dotted lines denote powered-off parts.

[0062] The signal of the gate line GATE jumps to the high level, the first driving control transistor T**1**, the second driving control transistor T**2** and the third driving control transistor T**3** are turned off, the gate voltage $V_{data}+V_{ref}+V_{th,DTFT}$ of the driving thin film transistor DTFT is held by the first capacitor C**1** and ensures that the driving thin film transistor operates in a saturation region. At this time, the output current I_d of the driving thin film transistor DTFT is:

$$\begin{aligned} I_d &= \frac{1}{2}\mu C_{ox}(W/L)(|V_{gs,DTFT}| - |V_{th}|)^2 \\ &= \frac{1}{2}\mu C_{ox}(W/L)[V_{dd} - (V_{data} + V_{ref} - V_{th}) - V_{th}]^2 \\ &= \frac{1}{2}\mu C_{ox}(W/L)(V_{dd} - V_{data} - V_{ref})^2. \end{aligned}$$

[0063] It can be seen from above that the current I_d flowing through the first electrode of the driving thin film transistor DTFT and the second electrode of the driving thin film transistor DTFT is independent of the threshold voltage $V_{th,DTFT}$ of the driving thin film transistor DTFT. Therefore a shift in the threshold voltage $V_{th,DTFT}$ of the driving thin film transistor DTFT would not affect a current output from the driving thin film transistor DTFT (that is, a drain current of the driving thin film transistor DTFT), so that the brightness of the light-emitting diode OLED would not be affected.

[0064] Meanwhile, during the light-emitting stage of the light-emitting diode OLED, the second light-emitting control transistor T**4** is turned on, so the current I_d flows into the light-emitting diode OLED through the second light-emitting control transistor T**4** and the light-emitting diode OLED emits light for display.

[0065] Furthermore, the low level of the initialization unit **30** may be grounded. If a voltage drop caused by a wiring resistor or a parasitic resistor exists on the high level input terminal ELVDD of the driving power supply, the low level of the initialization unit **30** may be adjusted such that it may offset the voltage drop caused by the wiring resistor or the parasitic resistor. In this case, the pixel circuit may further compensate the voltage drop caused by the wiring resistor or the parasitic resistor in the driving power supply, in order to

avoid fluctuations in the current I_d due to the voltage drop caused by the wiring resistor or the parasitic resistor.

[0066] In another aspect of the present disclosure, there is further provided an organic light-emitting display, wherein the organic light-emitting display comprises the above pixel circuit provided in the embodiments of the present disclosure. Since the pixel circuits may output uniform currents, the brightness of light-emitting diodes in the pixel circuits is uniform, and in turn the display brightness of the organic light-emitting display comprising the pixel circuits is uniform.

[0067] It may be understood that the implementations described above are only exemplary implementations utilized to explain the principle of the present disclosure, but the present disclosure is not limited thereto. For those ordinary skilled in the art, many variances and improvements may be made without departing from the spirit and essential of the present disclosure, and such variances and improvements are intended to be included in the scope sought for protection of the present disclosure.

1. A pixel circuit comprising a driving thin film transistor and a light-emitting diode, wherein the light-emitting diode is connected between a low level input terminal and a high level input terminal of a driving power supply in series, characterized in that the pixel circuit further comprises a first capacitor and a driving control unit, wherein a first terminal of the first capacitor is electrically connected with a first electrode of the driving thin film transistor through the driving control unit, a second terminal of the first capacitor is connected with a gate of the driving thin film transistor, a second electrode of the driving thin film transistor is electrically connected with the gate of the driving thin film transistor through the driving control unit, the driving control unit is connected with a gate line and a data line, and during a data writing stage, the driving control unit controls to connect the first terminal of the first capacitor to the first electrode of the driving thin film transistor and connect the gate of the driving thin film transistor to the second electrode of the driving thin film transistor, such that the driving thin film transistor is turned on.

2. The pixel circuit of claim **1**, characterized in that the pixel circuit further comprises a second capacitor, wherein a first terminal thereof is connected with the second terminal of the first capacitor, and a second terminal thereof is electrically connected with the data line through the driving control unit.

3. The pixel circuit of claim **2**, characterized in that the driving control unit further comprises a first driving control transistor, wherein a gate thereof is connected with the gate line, a first electrode thereof is connected with the data line, and a second electrode thereof is connected with the second terminal of the second capacitor.

4. The pixel circuit of claim **3**, characterized in that the pixel circuit further comprises an initialization unit for providing a low level, wherein the initialization unit is connected to the second terminal of the first capacitor and the first terminal of the second capacitor.

5. The pixel circuit of claim **4**, characterized in that the initialization unit comprises an initialization transistor, wherein a first electrode thereof is connected with the second terminal of the first capacitor and the first terminal of the second capacitor, a second electrode thereof is connected with the low level input terminal, and a gate thereof is connected with a reset signal input terminal.

6. The pixel circuit of claim **1**, characterized in that the driving control unit comprises a second driving control transistor and a third driving control transistor, wherein a gate of the second driving control transistor is connected with the gate line, a first electrode of the second driving control transistor is connected with the second electrode of the driving thin film transistor, a second electrode of the second driving control transistor is connected with the gate of the driving thin film transistor, a gate of the third driving control transistor is connected with the gate line, a first electrode of the third driving control transistor is connected with the first terminal of the first capacitor, and a second electrode of the third driving control transistor is connected with the first electrode of the driving thin film transistor.

7. The pixel circuit of claim **6**, characterized in that the pixel circuit further comprises a light-emitting control unit, wherein the light-emitting control unit is connected with a light-emitting control line and is capable of connecting the high level input terminal of the driving power supply to the first electrode of the driving thin film transistor, and/or connecting the low level input terminal of the driving power supply to the second electrode of the driving thin film transistor, according to a signal supplied from the light-emitting control line.

8. The pixel circuit of claim **7**, characterized in that the light-emitting control unit comprises a first light-emitting control transistor and a second light-emitting control transistor, wherein a gate of the first light-emitting control transistor is connected with the light-emitting control line, a first electrode of the first light-emitting control transistor is connected with the first electrode of the driving thin film transistor, a second electrode of the first light-emitting control transistor is connected with the high level input terminal of the driving power supply, a gate of the second light-emitting control transistor is connected with the light-emitting control line, a first electrode of the second light-emitting control transistor is connected with the second electrode of the driving thin film transistor, a second electrode of the second light-emitting control transistor is connected with an anode of the light-emitting diode, and a cathode of the light-emitting diode is connected with the low level input terminal of the driving power supply.

9. The pixel circuit of claim **13**, characterized in that the driving thin film transistor, the first driving control transistor, the second driving control transistor, the third driving control transistor, the initialization transistor, the first light-emitting control transistor and the second light-emitting control transistor are all P-type transistors.

10. An organic light-emitting display, characterized in that the organic light-emitting display comprises the pixel circuit of claim **1**.

11. The pixel circuit of claim **5**, characterized in that the driving control unit comprises a second driving control transistor and a third driving control transistor, wherein a gate of the second driving control transistor is connected with the gate line, a first electrode of the second driving control transistor is connected with the second electrode of the driving thin film transistor, a second electrode of the second driving control transistor is connected with the gate of the driving thin film transistor, a gate of the third driving control transistor is connected with the gate line, a first electrode of the third driving control transistor is connected with the first terminal of the first capacitor, and a second electrode of the third driving control transistor is connected with the first electrode of the driving thin film transistor.

12. The pixel circuit of claim **11**, characterized in that the pixel circuit further comprises a light-emitting control unit, wherein the light-emitting control unit is connected with a light-emitting control line and is capable of connecting the high level input terminal of the driving power supply to the first electrode of the driving thin film transistor, and/or connecting the low level input terminal of the driving power supply to the second electrode of the driving thin film transistor, according to a signal supplied from the light-emitting control line.

13. The pixel circuit of claim **12**, characterized in that the light-emitting control unit comprises a first light-emitting control transistor and a second light-emitting control transistor, wherein a gate of the first light-emitting control transistor is connected with the light-emitting control line, a first electrode of the first light-emitting control transistor is connected with the first electrode of the driving thin film transistor, a second electrode of the first light-emitting control transistor is connected with the high level input terminal of the driving power supply, a gate of the second light-emitting control transistor is connected with the light-emitting control line, a first electrode of the second light-emitting control transistor is connected with the second electrode of the driving thin film transistor, a second electrode of the second light-emitting control transistor is connected with an anode of the light-emitting diode, and a cathode of the light-emitting diode is connected with the low level input terminal of the driving power supply.

14. The organic light-emitting display of claim **10**, characterized in that the pixel circuit further comprises a second capacitor, wherein a first terminal thereof is connected with the second terminal of the first capacitor, and a second terminal thereof is electrically connected with the data line through the driving control unit.

15. The organic light-emitting display of claim **14**, characterized in that the driving control unit further comprises a first driving control transistor, wherein a gate thereof is connected with the gate line, a first electrode thereof is connected with the data line, and a second electrode thereof is connected with the second terminal of the second capacitor.

16. The organic light-emitting display of claim **15**, characterized in that the pixel circuit further comprises an initialization unit for providing a low level, wherein the initialization unit is connected to the second terminal of the first capacitor and the first terminal of the second capacitor.

17. The organic light-emitting display of claim **16**, characterized in that the initialization unit comprises an initialization transistor, wherein a first electrode thereof is connected with the second terminal of the first capacitor and the first terminal of the second capacitor, a second electrode thereof is connected with the low level input terminal, and a gate thereof is connected with a reset signal input terminal.

18. The organic light-emitting display of claim **10**, characterized in that the driving control unit comprises a second driving control transistor and a third driving control transistor, wherein a gate of the second driving control transistor is connected with the gate line, a first electrode of the second driving control transistor is connected with the second electrode of the driving thin film transistor, a second electrode of the second driving control transistor is connected with the gate of the driving thin film transistor, a gate of the third driving control transistor is connected with the gate line, a first electrode of the third driving control transistor is connected with the first terminal of the first capacitor, and a second electrode of the third driving control transistor is connected with the first electrode of the driving thin film transistor.

19. The organic light-emitting display of claim **18**, characterized in that the pixel circuit further comprises a light-emitting control unit, wherein the light-emitting control unit is connected with a light-emitting control line and is capable of connecting the high level input terminal of the driving power supply to the first electrode of the driving thin film transistor, and/or connecting the low level input terminal of the driving power supply to the second electrode of the driving thin film transistor, according to a signal supplied from the light-emitting control line.

20. The organic light-emitting display of claim **19**, characterized in that the light-emitting control unit comprises a first light-emitting control transistor and a second light-emitting control transistor, wherein a gate of the first light-emitting control transistor is connected with the light-emitting control line, a first electrode of the first light-emitting control transistor is connected with the first electrode of the driving thin film transistor, a second electrode of the first light-emitting control transistor is connected with the high level input terminal of the driving power supply, a gate of the second light-emitting control transistor is connected with the light-emitting control line, a first electrode of the second light-emitting control transistor is connected with the second electrode of the driving thin film transistor, a second electrode of the second light-emitting control transistor is connected with an anode of the light-emitting diode, and a cathode of the light-emitting diode is connected with the low level input terminal of the driving power supply.

* * * * *

专利名称(译)	像素电路和包括其的有机发光显示器		
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申请(专利权)人(译)	京东方科技集团股份有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司.		
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摘要(译)

提供像素电路和有机发光显示器。像素电路包括驱动薄膜晶体管和发光二极管，发光二极管串联连接在驱动电源的低电平输入端和高电平输入端之间，该像素电路还包括第一电容和驱动控制单元，第一电容的第一端通过驱动控制单元与驱动薄膜晶体管的第一电极电连接，第一电容的第二端与驱动薄膜晶体管的栅极，第二电极连接驱动薄膜晶体管的驱动控制单元通过驱动控制单元与驱动薄膜晶体管的栅极电连接，驱动控制单元与栅极线和数据线连接。由于各个像素电路可以输出均匀的电流，因此像素电路中的发光二极管的亮度是均匀的，并且包括像素电路的有机发光显示器的显示亮度是均匀的。